

## **IN THE CLAIMS**

Please rewrite claim 1 as follows:

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C<sup>1</sup> 1. (Thrice Amended) A semiconductor device comprising a silicon substrate, and a bipolar transistor having a collector well having a first conductivity-type, an internal base region having a second conductivity-type and received in said collector well and an emitter region having said first conductivity-type and received in said internal base region, a first annular isolation trench encircling said collector well, a second annular isolation trench encircling said first annular isolation trench, and an annular diffused region having said second conductivity-type disposed between said first annular isolation trench and said second annular isolation trench while being in contact with said first and second annular isolation trenches, said annular diffused region having only one layer of material laid on top of an entirety of said annular diffused region.

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## **REMARKS**

Claim 1 was rejected under 35 U.S.C. §112, first paragraph. In support thereof, the Examiner alleged that the feature of the “annular diffused region having only one layer of material laid on top of said annular diffused region” is shown as just an intermediate product. In an operational final structure, according to the Examiner, there will be more than one metallization layer formed over the annular diffused region.

The Examiner's rejection is apparently based on the fact that interconnects are not shown in the drawings of the present application. However, it is respectfully submitted that interconnects are not part of the operational final product of the present invention.